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#### AUTOMATED SOFTWARE PROTECTION FOR THE MASSES AGAINST SIDE-CHANNEL ATTACKS





























#### SOFTWARE COUNTERMEASURES





#### SOFTWARE COUNTERMEASURES





Electromagnetic emissions Power consumption

change this

Function's result

don't change this





change this

don't change this





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Issues	Our contributions
Countermeasures are usually <b>manually</b> applied	Automatic application of the countermeasure
Countermeasures are usually given for <b>particular</b> ciphers	Any code can be hardened
Target a <b>wide</b> range of platforms (be lightweight)	Use <b>static</b> memory allocation Allocation of a <b>realistic</b> size (don't waste memory) Use <b>specialized</b> code generation
An attacker may <b>write</b> on an <b>executable</b> memory section	Use the <b>specialization</b> of the generator to manage memory permissions
Hard to have a <b>good trade-off</b> between security and performance	Highly <b>configurable</b> → possible to find a trade-off



































#### OUTLINE

#### Background

- Side channel attacks
- Software countermeasures
- Code polymorphism

### • Automated application of code polymorphism

- Overview
- Code transformations used
- Memory management

#### • Experimental evaluation

- Performance evaluation
- Security evaluation



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#### **STATICALLY**



Main idea:

The annotated function is replaced by a wrapper and a generator



#### **STATICALLY**



Main idea: Each annotated function has its own generator (with shared code segments)



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#### **STATICALLY**





#### **STATICALLY**



#### RUNTIME



Main idea: At runtime, a new polymorphic instance is generated at each call



#### STATICALLY





Main idea: At runtime, a new polymorphic instance is generated <del>at each call</del> once in a while

How to find a good trade-off between security and performance? How to have variability in between generations?



#### **STATICALLY**



#### RUNTIME



Main idea: The size of polymorphic instances vary

How to allocate memory?



STATICALLY





STATICALLY





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add r4, r4, r5 xor r6, r5, r8	Register shuffling RANDOM general purpose register permutation r4r11  add r11, r11, r7 xor r8, r7, r5	Instruction shuffling independent instructions are emitted in a RANDOM order
Semantic variants	<b>Noise instructions</b>	Dynamic noise
replacement of an instruction by a <b>RANDOMLY</b> selected semantic variant	insertion of a <b>RANDOM</b> number of <b>RANDOMLY</b> chosen noise instructions	RANDOM insertion of noise instructions with a RANDOM jump
add r4, r4, r5 xor r6, r5, #12348 xor r6, r6, r8	add r4, r4, r5 sub r7, r6, r2 load r3, r10, #53 instructions	add r4, r4, r5 jump 0, 1 or 2 instructions sub r7, r6, r2



Period of regeneration ℕ	Register shuffling {0, 1}	Instruction shuffling {0, 1}	
Semantic variants	Noise instructions	Dynamic noise	
<b>{0, 1, 2</b> }	$\{0,1,2\} imes\mathbb{R} imes\mathbb{N}$	$\mathbb{N}$	
Total configuration space: $\{0, 1\}^2 \times \{0, 1, 2\}^2 \times \mathbb{R} \times \mathbb{N}^3$			



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#### **STATICALLY**



#### RUNTIME



Main idea: The size of polymorphic instances vary

How to allocate memory?



Amount of used memory





#### **OVERFLOW PREVENTION**

#### STATICALLY





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Objective: Guarantee W  $\oplus$  X and that only the generator can write into the buffer





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#### **EXPERIMENTAL SETUP**

• 15 different test cases

#### 4 different selected configurations

- none: no polymorphism
- IOW: only noise instructions, generation is done every 250 executions
  - Theoretical number of variants is already very high!
    >6×10<sup>22</sup> variants for a 10 instructions code
    >10<sup>704</sup> variants for the 278 instructions AES we use
- medium: all transformations activated, generation is done every execution
- high: all transformations activated, different probability model for noise instructions insertion, generation is done every execution

#### • STM32 board (ARM cortex M3 – 24 MHz – 8kB of RAM)





Configuration	Execution time overhead (geometric mean)	Size overhead (geometric mean)
none 🗖	x1.40	x1.70
low 🔹	x2.31	x2.87
medium 🔻	x2.45	x3.44
high 🔺	x4.03	x3.81



Number of original instructions generated



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CPA on Sbox output with HW

290 traces for unprotected AES

3 800 000 traces for configuration low

Success rate at 0.8 in

## **SECURITY EVALUATION**

Technical details: PicoScope 2208A, EM probe RF-U 5-2 (Langer), PA 303 preamplifier (Langer) Sampling at 500 Msample/s with 8bits resolution, 24500 samples per trace



## Ceatech

## CONCLUSION

- Automatic ?
- Configurable 🛛
- Efficient 🛛
- With static memory allocation of a realistic size ?
- With memory permission management ?
- Usable on constrained devices ?
- Open question: interest of code polymorphism against fault injection attacks?



RUNTIME



Automated software protection for the masses against side-channel attacks

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# Thank you for your attention

**Questions?** 

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AGENCE MATIONALE DE LA RECHERCHE

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